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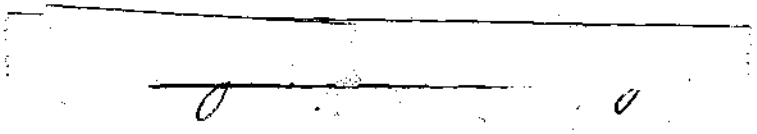

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FIELD EFFECT TRANSISTORS
IN DIFFERENTIAL AMPLIFIERS

A Thesis

Presented to

The Faculty of the Graduate Division

by

James S. Gray

In Partial Fulfillment

of the Requirements for the Degree

Master of Science in Electrical Engineering

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FIELD EFFECT TRANSISTORS

IN DIFFERENTIAL AMPLIFIERS

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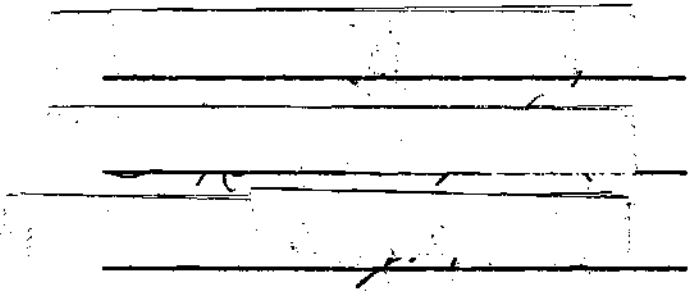

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SUMMARY

The performance of field effect transistors (FET's) is predicted and evaluated in direct-coupled differential amplifiers. Two advantages of the FET are its low noise and high input impedance. For direct-coupled differential amplifiers the limiting factor to sensitivity is drift due to temperature. It is shown theoretically that it is possible to predict a value of quiescent drain current, at which the change of drain current with temperature is a minimum. This property is verified experimentally for a sample of 10 FET's. The equivalent input drift of a FET differential stage can be minimized, therefore, not only by matching the two FET's but also by proper choice of the quiescent value of drain current. The equivalent input drift for a differential stage using the most closely matched pairs of the 10 FET's is evaluated.

At low values of drain current where drain-source resistance is large it is shown theoretically that the FET differential stage is capable of high common mode rejection. This is verified experimentally.

CHAPTER I

INTRODUCTION

Differential amplifiers represent a special class of amplifiers whose function is to amplify only the difference between two signals regardless of each signal's potential with respect to the amplifier ground. The development of such amplifiers was necessary for measurements in the behavioral sciences, general measurements instrumentation, and now telemetry.

For an example, which illustrates the need for differential amplification, consider Figure 1. In the transducer bridge, f(R)

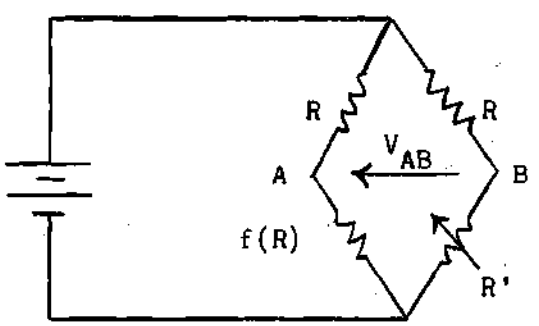


Figure 1. Transducer Bridge.

is a resistance whose value depends upon some environmental parameter that one wishes to measure, e.g. pressure, light, heat, etc. The desired output voltage, V_{AB}, is obviously floating with respect to the power supply ground. Thus, an amplifier with a floating input is required. It is also seen that the amplifier may have voltages

at points A and B to ground that are several orders of magnitude larger than the desired difference in potential between A and B. These voltages, known as common mode voltages, also have components due to such things as variations of the power supply output, ground loops due to long cables, and electromagnetic phenomena. Thus, the amplifier must amplify the weak voltage between the two input terminals but discriminate strongly against the large voltages common to both input terminals.

Differential amplifiers are also used in electroencephalography. Amplification of the voltage between two electrodes attached to the scalp is desired, but spurious results are likely to be produced if single-ended amplification is attempted. This is due to interference introduced into the signal source, the most prominent of which are 60 cycle signals due to the surroundings. The solution to this problem consists of using a high input impedance differential amplifier. The interference signal appears at both input terminals and is therefore not amplified.

A classic example of such an amplifier is shown in Figure 2. This circuit has a floating input and output. Two types of input and output signals are defined, i.e. common mode and differential mode. The common mode (CM) signal is defined as the average of the voltages of the two terminals with respect to ground. The differential mode (DM) signal is defined as half the difference between the voltages. If both tubes have identical μ and r_p, then by use of the bisection theorem[1] the following formulas may be derived.

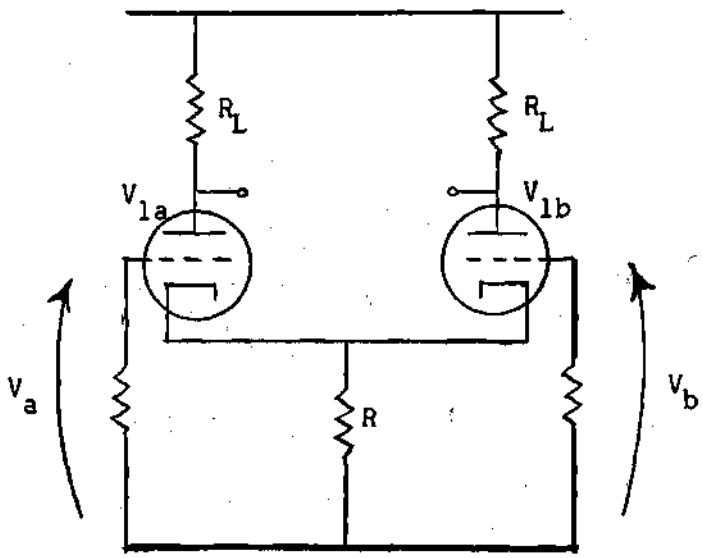


Figure 2. Vacuum Tube Differential Amplifier.

$$\frac{V_{1a} + V_{1b}}{2} = \frac{-\mu R_L}{R_L + r_p + 2R(1 + \mu)} \frac{V_a + V_b}{2}$$

$$\frac{V_{1a} - V_{1b}}{2} = \frac{-\mu R_L}{R_L + r_p} \frac{V_a - V_b}{2}$$

It is seen from the above that the CM output $\frac{V_{1a} + V_{1b}}{2}$ is only a function of the CM input $\frac{V_a + V_b}{2}$. A similar statement is true for the DM signals. Moreover, it is seen that the CM gain is less than the DM gain. In fact, as $R \rightarrow \infty$ the CM gain approaches zero. Thus, the previously discussed requirement for making the DM gain much greater than the CM gain can be achieved. A practical method of making dynamic R large is to use a constant current pentode instead of R.

In practice, the active amplifying elements are not exactly

matched. Under this realistic condition, the following equations may be written for the above amplifier or for any differential amplifier.

$$\left(\frac{V_{1a} - V_{1b}}{2}\right) = \alpha\left(\frac{V_a - V_b}{2}\right) + \beta\left(\frac{V_a + V_b}{2}\right)$$

$$\left(\frac{V_{1a} + V_{1b}}{2}\right) = \gamma\left(\frac{V_a - V_b}{2}\right) + \delta\left(\frac{V_a + V_b}{2}\right)$$

From these equations, it is seen that a CM input produces both a CM output and a DM output. Likewise, a DM input produces both a DM and a CM output. Therefore, it is not possible to predict whether the DM output was due to the desired DM input or to a CM input α/β times the DM value. Since the CM voltages are very often many orders of magnitude larger than the DM input voltages, the results of unbalances can be quite serious. Therefore, it is convenient to define several quality factors for a differential amplifier. These are as follows:

1. $$H = \frac{\alpha}{\beta}$$

H is called the "rejection factor" and is the ratio of CM and DM signals at the input terminals which cause the same DM output

$$H = \frac{(V_{1a} - V_{1b})\Big|_{V_a = -V_b = k}}{(V_{1a} - V_{1b})\Big|_{V_a = V_b = k}}$$

2. $$F = \frac{\alpha}{\delta}$$

F is called the "discrimination factor" and is the ratio of the total DM amplification to the total CM amplification

or
$$F = \frac{(V_{1a} - V_{1b})\Big|_{V_a = -V_b = k}}{(V_{1a} + V_{1b})\Big|_{V_a = V_b = k}}$$

Additional quality factors may be defined, but the above two are normally regarded as the important ones.

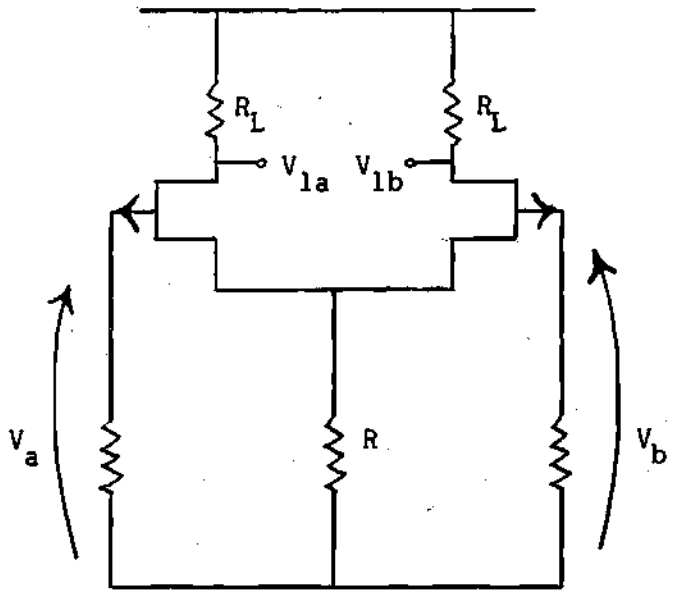
If the preceding circuit is solved under the conditions that $\mu_1 = \mu + \delta\mu$ and $\mu_2 = \mu - \delta\mu$, $r_{p1} = r_p + \delta r_p$ and $r_{p2} = r_p - \delta r_p$, etc.,[2] it is found that, if R approaches infinity, H and F assume the following values:

$$(H \text{ min.})\Big|_{R=\infty} = \frac{\partial\mu}{\delta\mu}$$

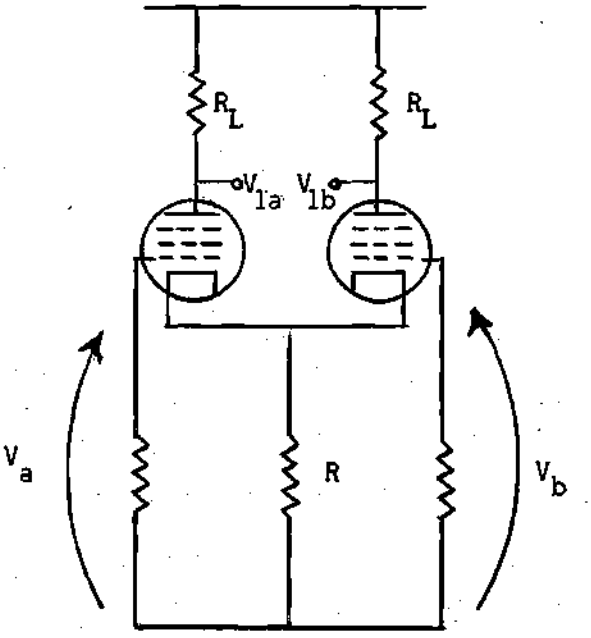
$$F\Big|_{R=\infty} = \infty$$

Thus as R approaches infinity, the discrimination factor approaches infinity but H approaches a finite value which is related to the amount of unbalance in the active devices' parameters. In a typical case H usually approaches a value of several thousand which may be entirely inadequate since the CM inputs may be 10^5 or 10^6 times the DM inputs. With no feedback between stages, it can be shown that the overall rejection factor of a multiple stage differential amplifier is essentially that of the first stage.

The effect of unbalances on the rejection factor of the differential stages in Figure 3 will now be calculated. In Figure 3 the active elements are field effect transistors in one stage and pentodes in the other. At low frequencies, the small signal models are the same.



Field Effect Transistor Differential Stage



Pentode Differential Stage

Figure 3. FET and Pentode Differential Stages

(Biasing circuits not shown for simplicity)

This model is shown in Figure 4. The common mode rejection factor under

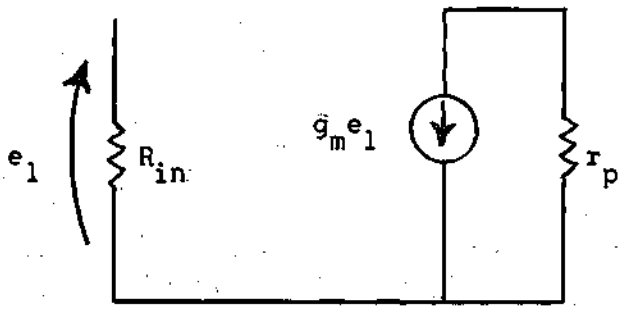


Figure 4. Small Signal Low Frequency Model for Field Effect Transistor or Pentode.

the condition that r_p approaches infinity assumes the following form(3)

$$H\Big|_{r_p \to \infty} = \frac{(1 + 2g_m R)2m}{\delta g_m}$$

Therefore, if R approaches infinity, H will approach infinity and one finally has the desired results of both H and F approaching infinity. The above condition of r_p being very large can be met by a good quality pentode or by a field effect transistor at small values of drain current. A similar analysis of a regular transistor differential stage shows that H approaches infinity as R approaches a finite but very large value.

It should be noted at this time that these results are valid only for small signal operation and values of the DM and CM inputs such that the devices remain in their linear regions.

The frequency range of most physical phenomena, for which

differential amplification is required, lies from DC to about one thousand cps. When amplification of very low frequencies is required, additional difficulties arise. First, all active devices have parameters which are dependent on temperature and other environmental factors. Second, at low frequencies of operation all active devices suffer from $1/f$ noise effects which degrades the signal to noise ratio. There are two possible solutions to the above difficulties. One is to use low noise active devices in direct coupled differential amplifiers in such a manner that drift effects due to temperature are minimized. The other is to use suppressed carrier amplification techniques in which the low pass signal is converted into a band pass signal. A short discussion of the advantages and disadvantages of each approach is presented below:

In direct coupled differential amplifiers one has the problem of not being able to determine whether a change in voltage at the output was due to the presence of the desired DM input signal or to a change in ambient temperature. It is convenient, therefore, to define a quality factor known as the equivalent input drift which has units of volts/°C and/or amp/°C. This quality factor indicates that value of DM input which would produce the same output voltage change as a one degree centigrade temperature change. A knowledge of the temperature range to which the amplifier will be subjected and the equivalent input drift enable one to decide the minimum value of DM input voltage which can be reliably measured. This change in the output due to temperature has turned out to be the main limiting factor, rather than noise, on the sensitivity of direct coupled amplifiers.

Thus, when using low noise active devices of such a nature that F and H can approach infinity in the above amplifiers, the main design emphasis become that of reducing the equivalent input drift. The advantages of such a system over a suppressed carrier system is that it is a much simpler system employing significantly fewer components, both active and passive. Suppressed carrier systems also suffer from spikes and intermodulation distortion.

In a suppressed carrier differential amplifier the inputs are converted from low pass to band pass signals. The actual amplifier is strictly an a-c amplifier which eliminates any drift problems due to temperature. The center frequency of operation can be picked such that noise figure is optimized. All the design problems are now concerned with spurious signals produced by the modulator or chopper. There are error voltages associated with both the on and off states of the choppers. Since the suppressed carrier system consists of a modulator, ac differential amplifier, demodulator, and low pass filters, it will in general be more complex than an equivalent direct-coupled system. Some of the separate subsystems, however, are easier to design since they are ac small signal circuits.

With the present level of technology, the suppressed carrier amplifier is passing from the scene. By using well matched transistors and the appropriate circuitry the equivalent input drift of direct-coupled differential amplifiers has been reduced to the level of the offset voltages associated with the best choppers. Since, such an amplifier is much simpler than an equivalent suppressed carrier system, most differential amplifiers presently being manufactured.

for general measurements are direct coupled.

The field effect transistor (FET) has several characteristics which make it look attractive as both an amplifying element in direct-coupled differential amplifiers and a modulator in suppressed carrier systems. It is the purpose of this investigation to predict and evaluate the performance of FET's only in the direct-coupled differential amplifier.

The silicon function FET has a dynamic DC gate-source resistance of about 10^9 ohms. In fact, except for almost zero frequency signals, the limit to the input impedance is the capacitance at the input. The differential stage is ideal for simple intrastage feedback which can reduce the input capacitance significantly. Thus, very high input impedances can be achieved. The typical transistor differential amplifier has a differential input impedance ranging from about 500,000 ohms to a maximum of 10 megohms. Thus, the FET differential stage is inherently capable of a much higher DM input impedance than the transistor differential stage.

The FET is a low noise device. It has been shown theoretically that at low frequencies the FET has a lower noise figure than tubes or regular transistors. This is primarily due to the fact that the FET is a majority carrier device.

The dominant drift parameters for FET'S are of such a nature that at an operating point, which can be predicted, their effects on the drain current tend to cancel. This will be shown in the following chapter. Thus, the equivalent input drift can be reduced, not only by matching the two FET's but also by proper choice of the quiescent

operating point.

As shown previously, the FET differential stage is also capable of very high common mode rejection. The FET, therefore, has advantages over other existing active elements in the direct-coupled differential stage.

CHAPTER II

THE MINIMIZATION OF TEMPERATURE EFFECTS ON FET'S

The equations giving the behavior of FET's in the pinched off region (see Figure 5) have been developed in several classic papers. The first expression which was derived by Shockley[4] has the form

$$I_D = I_{DSS}\left[1 - 3\frac{V_{GS}}{V_p} + \left(\frac{V_{GS}}{V_p}\right)^{3/2}\right]$$

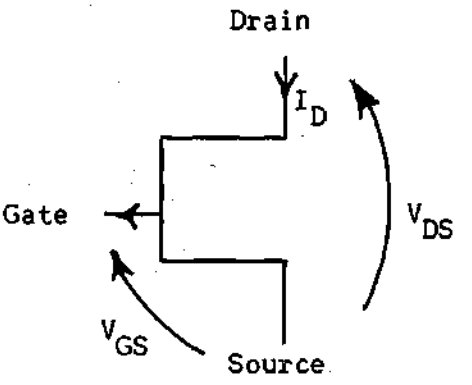
This equation was derived assuming a step junction and holds for alloy junction field effects. In FET's made by a diffusion process the longitudinal electric field exceeds 1000 V/cm and carrier mobility becomes proportional to the square root of the electric field. Shockley's equation assumes that the mobility remains constant. Dacey and Ross[5] derived the following expression for this case.

$$I_D = I_{DSS}\left\{4\left[1 - \left(\frac{V_{GS}}{V_p}\right)^{1/2}\right]^3 - 3\left[1 - \left(\frac{V_{GS}}{V_p}\right)^{1/2}\right]^4\right\}^{1/2}$$

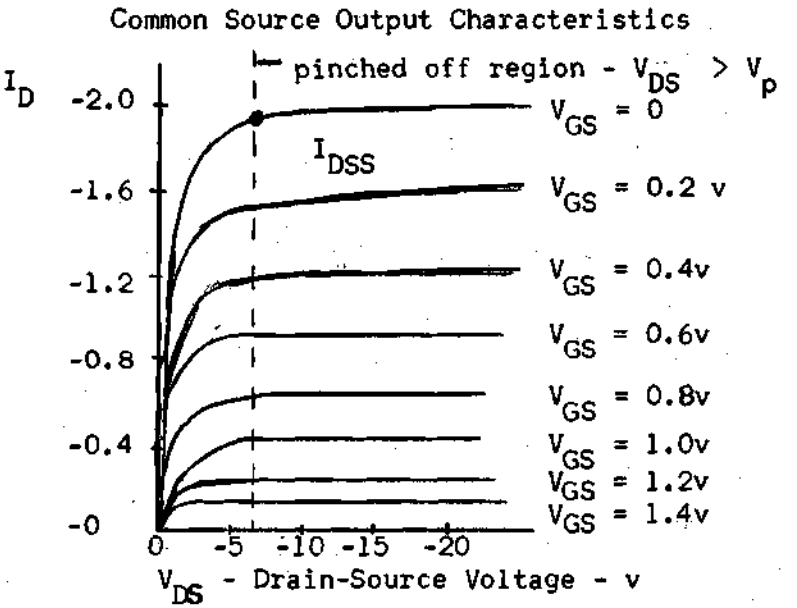
Most junction FET's are now made by the diffusion process.

Middlebrook and Richer,[6] however, have shown that the behavior of the FET for all junction shapes is more accurately and simply described by the following equations

$$I_D = I_{DSS}\left(\frac{V_{GS}}{V_p} - 1\right)^N \qquad (1)$$



Symbol for Silicon p Channel FET



$I_{DSS} \triangleq I_D$ at some specified V_{DS} in the pinched-off region when $V_{GS} = 0$.

g'_{fs} = value of small signal low frequency y_{21} parameter at $V_{GS} = 0$ and V_{DS} some specified value in the pinched-off region.

$g_{fs} = \frac{\partial I_D}{\partial V_{GS}}$ at any operating point

$I_o = 0$ when $V_{GS} = V_p$

Figure 5. Terminology and Typical Characteristics of a FET.

$$V_p = \frac{NI_{DSS}}{g'_{fs}} \tag{2}$$

$$g_{fs} = \frac{\partial I_D}{\partial V_{GS}} = g'_{fs}\left(\frac{V_{GS}}{V_p} - 1\right)^{N-1} \tag{3}$$

$$2 \leq N \leq 2.25 \quad \text{Normally} \quad N = 2$$

These equations hold quite well for manufactured diffusion process FET's as illustrated in Figure 6.

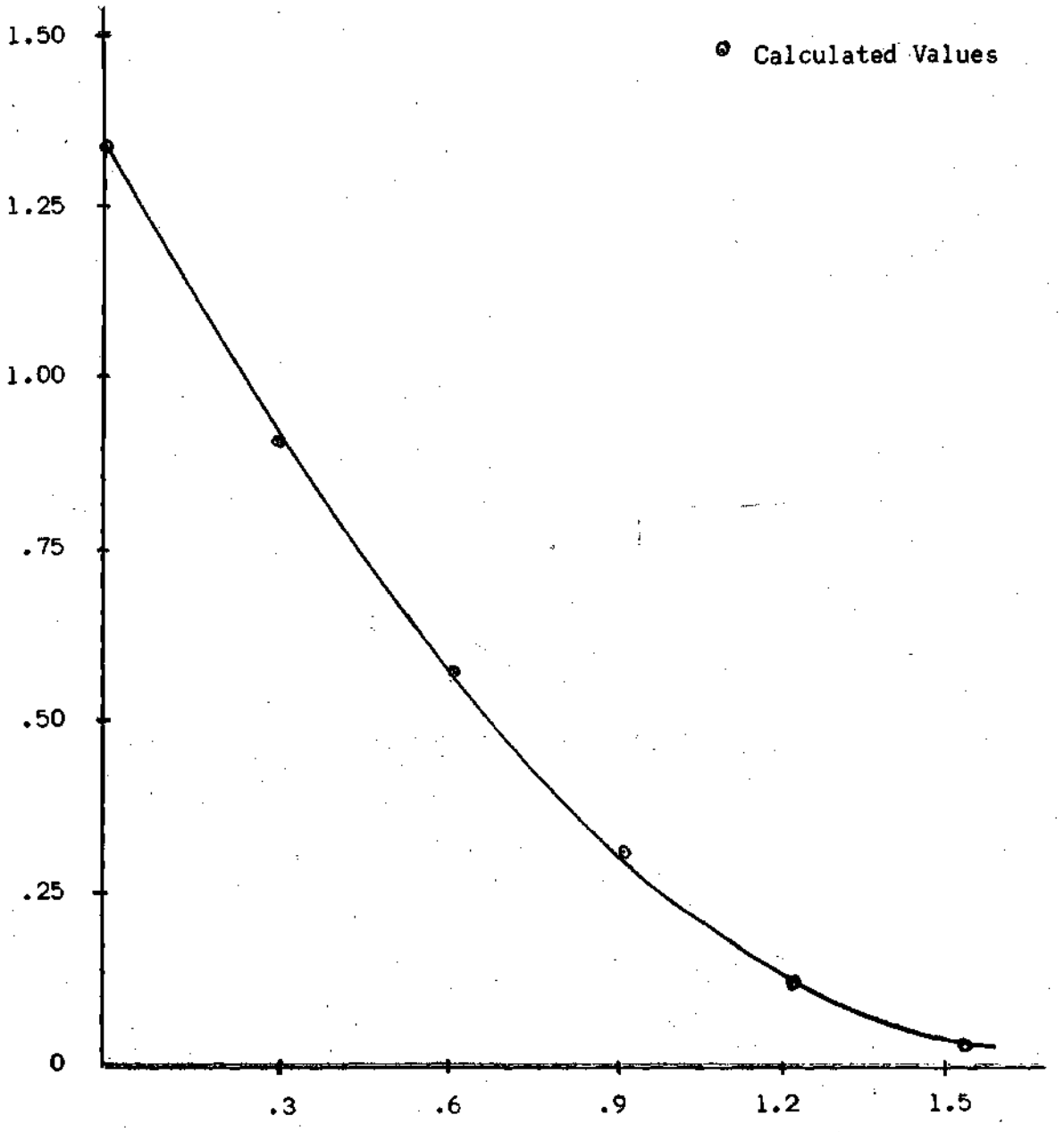
The effect of temperature upon the drain current can be shown by several different approaches. One is to write the drain current equation in terms of I_{DSS} and g'_{fs}, both of which are temperature dependent. The change of these quantities with temperature is non-linear. In the region from 0 to 50 degrees centigrade, however, it can be seen from Figure 7 and Figure 8 that the curves are fairly linear and may be approximated closely by the following equations:

$$\frac{I_{DSS}}{I_{DSS}\big|_{T \text{ reference}}} = 1 - k\tau \tag{4}$$

$$\frac{g'_{fs}}{g'_{fs}\big|_{T \text{ reference}}} = 1 - c\tau \tag{5}$$

where $\tau = T - (T \text{ reference})$ in degrees centigrade.

When equations (3), (4), and (5) are substituted in equation (1), and the derivative of equation (1) with respect to τ is set equal to zero, the value of the gate-source voltage, which makes this derivative equal to zero, is found to be



$$I_D = I_{DSS} \left(\frac{V_{GS}}{V_p} - 1 \right)^2$$

$I_{DSS} = 1.34$ ma

$V_p = 1.75$ volts

Figure 6. Calculated I_D Superimposed upon Experimental I_D versus V_{GS} Curve for 2N2497 - Specimen A.

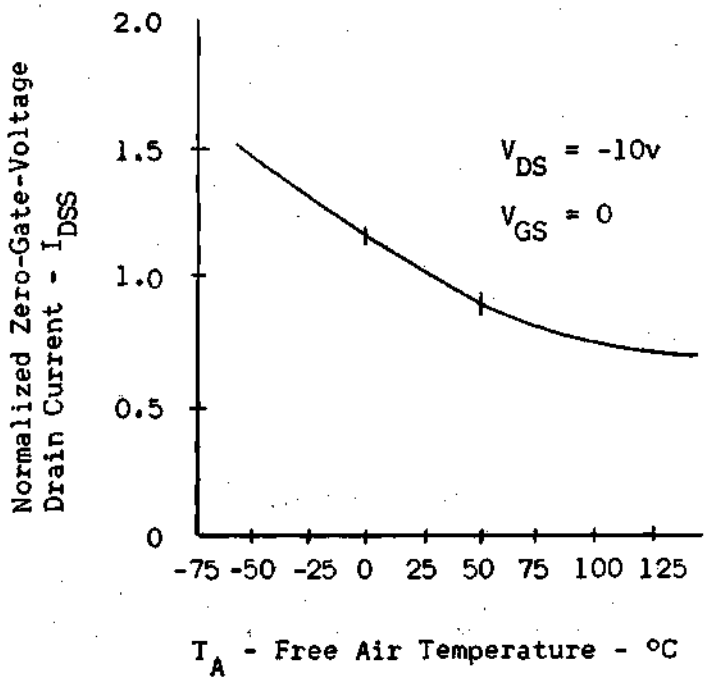


Figure 7. Normalized Zero-Gate-Voltage Drain Current vs Free-Air Temperature.

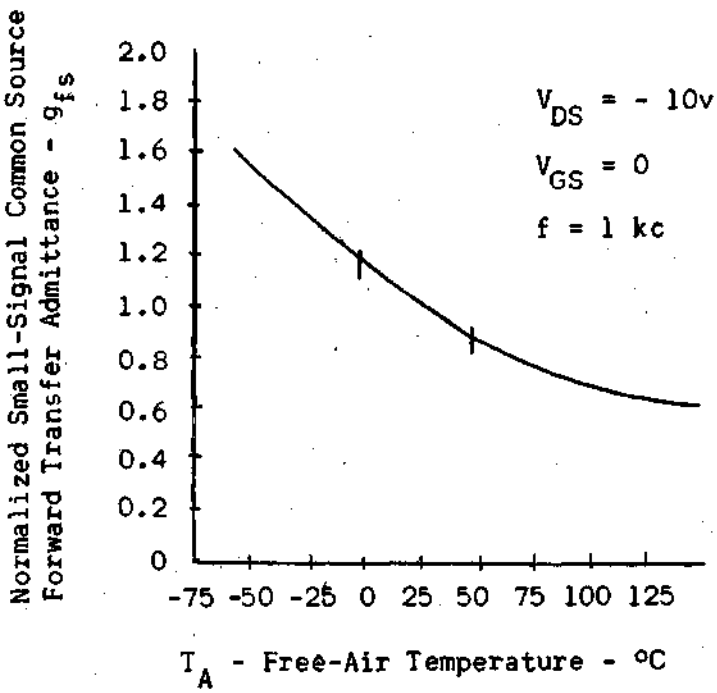


Figure 8. Normalized Small-Signal Common-Source Forward Transfer Admittance vs Free-Air Temperature.

$$V_{GS} = \frac{I_{DSS}|_{T\ reference} + k(1 - k\tau)}{g'_{fs}|_{T\ reference} \quad CI_{DSS}|_{T\ reference} + (1-k\tau) - 1/2kI_{DSS}g'_{fs}|_{T\ reference} \quad (1-c\tau)}$$

Thus, the value of V_{GS} which results in zero drift is temperature dependent and one cannot, therefore, obtain exactly zero drift. k and c, however, are both small and normally fairly close numerically. The above expression for V_{GS} is fairly constant then over the range of temperature considered.

In other words

$$V_{GS} \approx \frac{I_{DSS}|_{T\ ref.}^{\ k}}{g'_{fs}|_{T\ ref.} \quad c\ I_{DSS}|_{T\ ref.} - 1/2\ k\ I_{DSS}|_{T\ ref.} \quad g'_{fs}|_{T\ ref.}}$$

which simplifies to

$$V_{GS} \approx \frac{k}{2c - k} \quad V_p|_{T\ ref.} \tag{8}$$

Since the operating point in a differential stage would be set by a current source common to both FET's source terminals, the preceding equation is substituted in equation (1) to find the value of quiescent I_D which gives minimum drift. The result is

$$I_D = I_{DSS}\, 4\left(\frac{k - c}{2c - k}\right)^2 \tag{9}$$

The value of quiescent I_D or V_{GS} to give minimum drain current change with temperature can also be found by considering the temperature dependence of I_{DSS} and V_p. As before the temperature dependence of I_{DSS} is linearized over the region from 0°C to 50°C to be

$$I_{DSS} = I_{DSS}\big|_{T\ ref.} (1 - k\tau) \tag{10}$$

$\tau = T - (T\ ref.)$ in degrees centigrade

The temperature dependence of V_p is well established and is due to the temperature dependence of the contact potential. V_p as a function of temperature may be written

$$V_p = V_p\big|_{T\ ref.} + 2 \times 10^{-3}\tau \tag{11}$$

$$\tau = T - T\ ref.$$

Setting the derivative of equation (11) with respect to τ equal to zero yields

$$\frac{\partial I_D}{\partial \tau} = 0 = \frac{\partial I_{DSS}}{\partial \tau}\left(\frac{V_{GSS}}{V_p} - 1\right) - 2I_{DSS}\frac{V_{GS}}{V_p^2}\frac{\partial V_p}{\partial \tau} \tag{12}$$

Solving for V_{GS} in the above equation yields

$$V_{GS} = \frac{k'V_p^2}{4 + k'V_p} \tag{13}$$

$k' = 10^3 k$

or

$$V_{GS} \approx \frac{k'V_p^2\big|_{T\ ref.}}{4 + k'V_p\big|_{T\ ref.}} \tag{14}$$

Equation (14) is substituted into equation (1) to find the quiescent value of I_D giving minimum drift. This result is

$$I_D = I_{DSS}\left(\frac{-4}{4 + k'V_p|_{T\ ref.}}\right)^2 \qquad (15)$$

$$k' = 10^3 k$$

Two expressions giving quiescent I_D for minimum drift have been derived, namely equations 9 and 15. The relationship between the two expressions will be shown in the following manner. Assuming the dependence of I_{DSS} with temperature to be linear over the region of interest and using the temperature dependence of V_p, the change of g_{fs} with temperature is found from equation (2).

$$g'_{fs} = \frac{2I_{DSS}}{V_p}$$

Now

$$\frac{g'_{fs}}{g'_{fs}|_{T\ ref}} = \frac{\frac{2I_{DSS}}{V_p}}{\frac{2I_{DSS}|_{T\ ref}}{V_p|_{T\ ref}}} = \left(\frac{V_p|_{T\ ref}}{V_p}\right)\left(\frac{I_{DSS}}{I_{DSS}|_{T\ ref}}\right)$$

From previous derivations

$$\frac{V_p|_{T\ ref}}{V_p} = 1 - \frac{2 \times 10^{-3}}{V_p}\tau$$

$$\approx 1 - \frac{2 \times 10^{-3}}{V_p|_{T\ ref}}\tau$$

$$\frac{I_{DSS}}{I_{DSS}|_{T\ ref}} = 1 - k\tau$$

Let

$$A = \frac{2 \times 10^{-3}}{V_p|_{T\ ref}}$$

$$\frac{g'_{fs}}{g'_{fs}|_{T\ ref}} = (1 - A\tau)(1 - k\tau)$$

$$= 1 - (A + k)\tau + Ak\tau^2$$

$$= 1 - (A + k - Ak\tau)\tau$$

Now k normally equals about 5×10^{-3}, $A \approx 10^{-3}$, and τ maximum equals 25°C so that above is approximately

$$\frac{g'_{fs}}{g'_{fs}|_{T\ ref}} \approx 1 - (A + k)\tau$$

which verifies our original assumption in the first derivation that

$$\frac{g'_{fs}}{g'_{fs}|_{T\ ref}} = 1 - c\tau$$

Hence

$$c \approx k + A$$

$$c = k + \frac{2 \times 10^{-3}}{V_p} \qquad (16)$$

If the value of c given in equation 16 is now substituted into equation 9 the result is

$$I_D = I_{DSS}4\left(\frac{k - k - \frac{2 \times 10^{-3}}{V_p}}{2k + \frac{4 \times 10^{-3}}{V_p} - k}\right)^2 \qquad (17)$$

Equation 17 reduces to

$$I_D = I_{DSS}\left(\frac{-4}{k'V_p + 4}\right)^2$$

$$k' = 10^3 k$$

which is precisely equation 15, the alternate equation giving the quiescent I_D for minimum drift.

CHAPTER III

INSTRUMENTATION AND PROCEDURE

In order to evaluate the effect of temperature variation on FET performance, some type of regulated temperature oven was required. Due to the symmetry of the device parameter change about room temperature, it was decided to experimentally analyze the drift properties of FET's only in the region from room temperature to 50 degrees centigrade. For this purpose, the following temperature oven was constructed

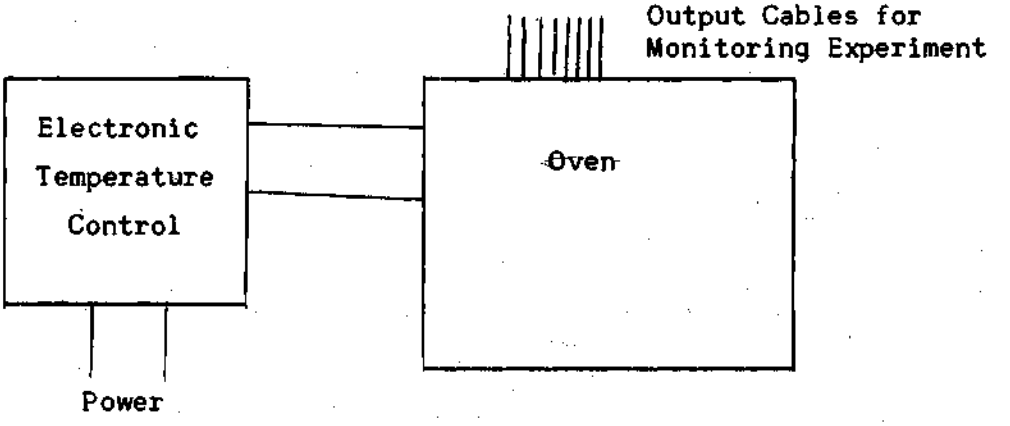


Figure 9. Temperature Oven

The actual oven is a 13" x 10.5" x 3.5" plastic box with 40 two watt 6800 ohm resistive heaters mounted around the sides and connected in parallel electrically. An eight conductor cable with a Cinch-Jones connector was attached to the bottom of the box. These cables were data transmission and power lines for the components in the box. The electronic

temperature control is shown in Figure 10.

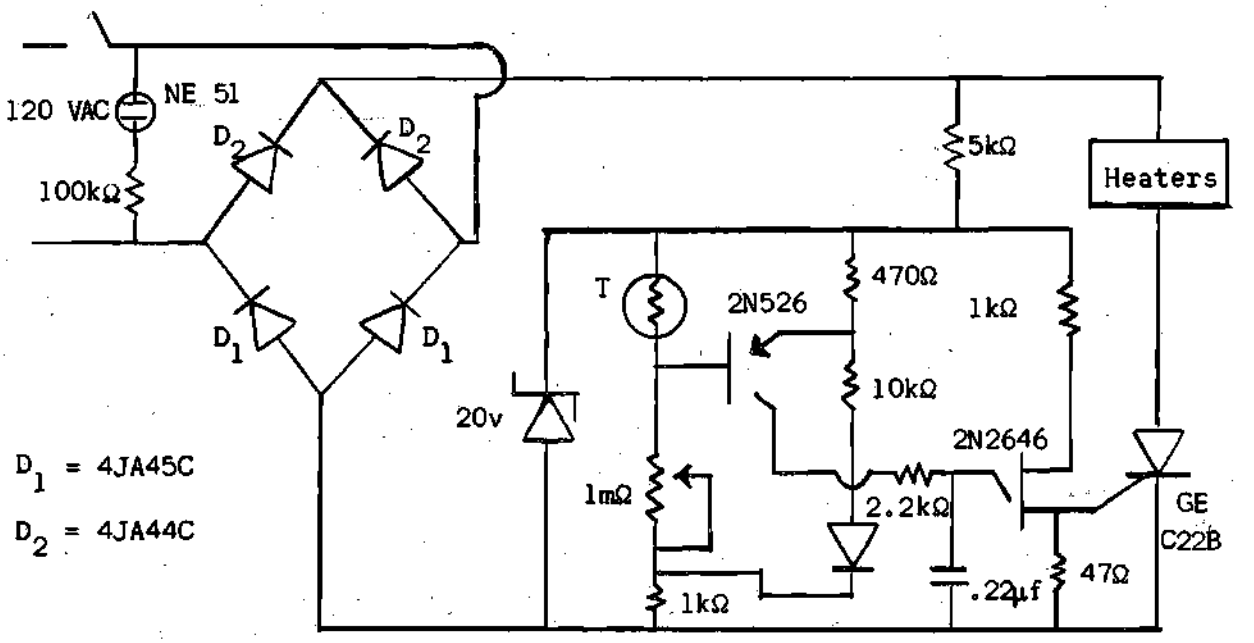


Figure 10. Electronic Temperature Control.

For any setting of the one megohm potentiometer there is an equilibrium temperature for the oven at which the thermistor value and pot value of resistance make the SCR conduct for the proper portion of each cycle such that this temperature is maintained fixed.

The experimental setup for measuring drain current versus temperature for various gate source voltages and fixed drain-source voltage is shown in Figure 11. Drain-source and gate-source voltages are derived from Hewlett-Packard Model 721A regulated power supplies. The gate-source voltage is varied from zero to three volts in ten equal increments by the precision voltage divider. Since the gate-source leakage current I_{GSS} is approximately one nano-ampere for the bias conditions shown, switching the gate to various positions on the voltage divider does not load the

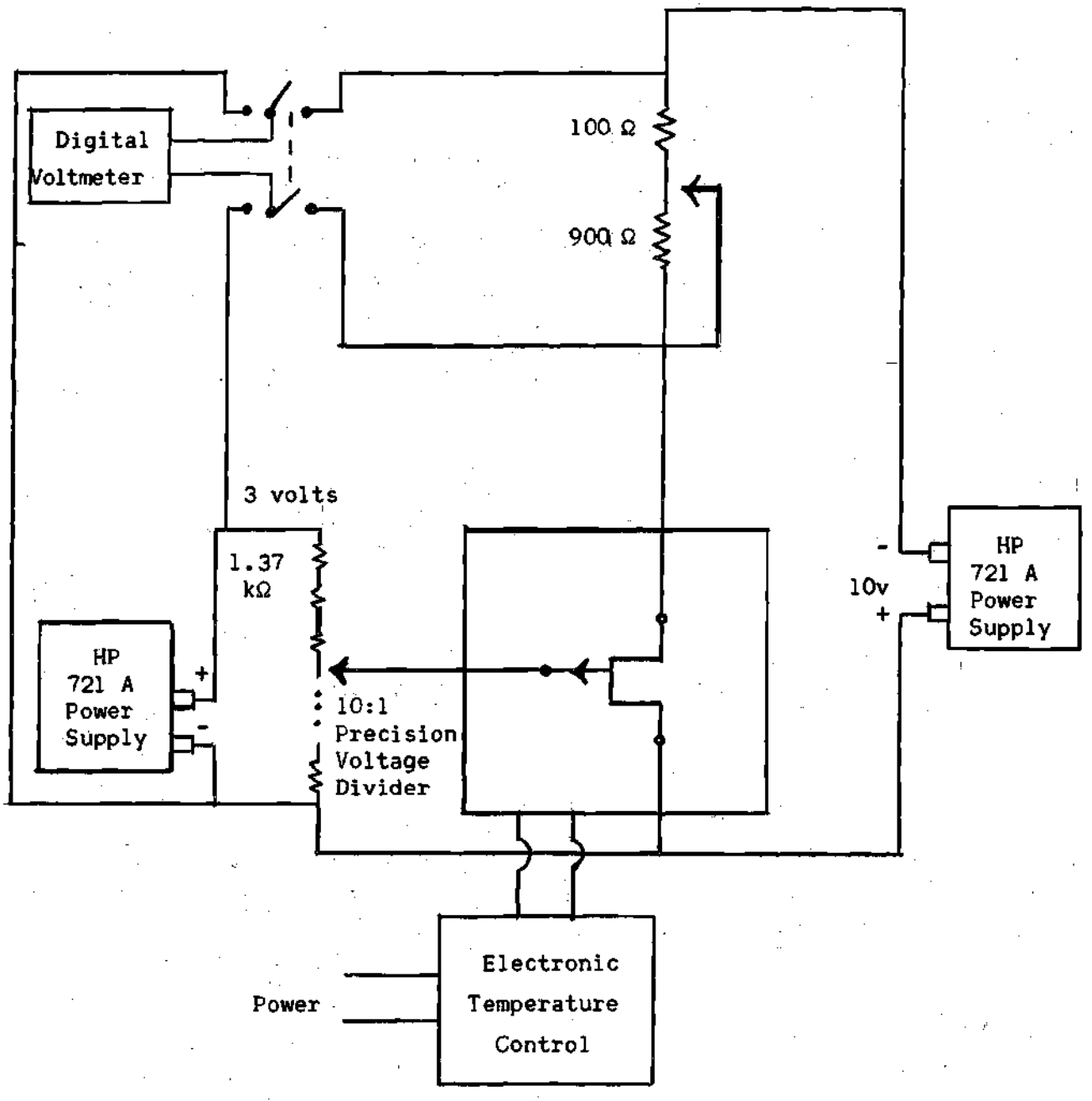


Figure 11. I_D Versus V_{GS} and Temperature Measurement Setup.

divider enough to cause any measurable change from the unloaded values. The digital voltmeter can be switched to read the voltage across the divider or to measure the voltage across a 100 or 1000 ohm resistor in the drain current circuit. For higher current values the voltage across the 100 ohm resistor is used to measure drain current. At lower levels this resistance is increased to 1000 ohms to give more accuracy in the readings.

Drain current was measured for various gate-source voltages at room temperature, which was 22°C, and at 50°C for a sample of 10 FET's. The statistical average of many runs for the 10 FET's is included in the Appendix.

Next, the most closely matched pairs were used in a differential stage and the equivalent input drift measured. The experimental apparatus to measure equivalent input drift is shown in Figure 12. The 2N2905 transistor acts as a current source to bias the FET's. Rotation of the potentiometer wiper varies the collector current. This transistor also acts as a high dynamic resistance to current changes and produce feedback to offset possible changes. If the FET's were perfectly matched, there would be no change with temperature of the differential output. The equivalent input drift is, therefore, strictly a function of the difference in the drift parameters of the FET's.

The load resistances can be varied by the potentiometer connection shown to give zero offset at the reference temperature. The temperature is changed ΔT degrees and the millivac suppressed carrier DC voltmeter measures the DM voltage change. This change, divided by the DM gain for the particular values of drain current and load resistances, and

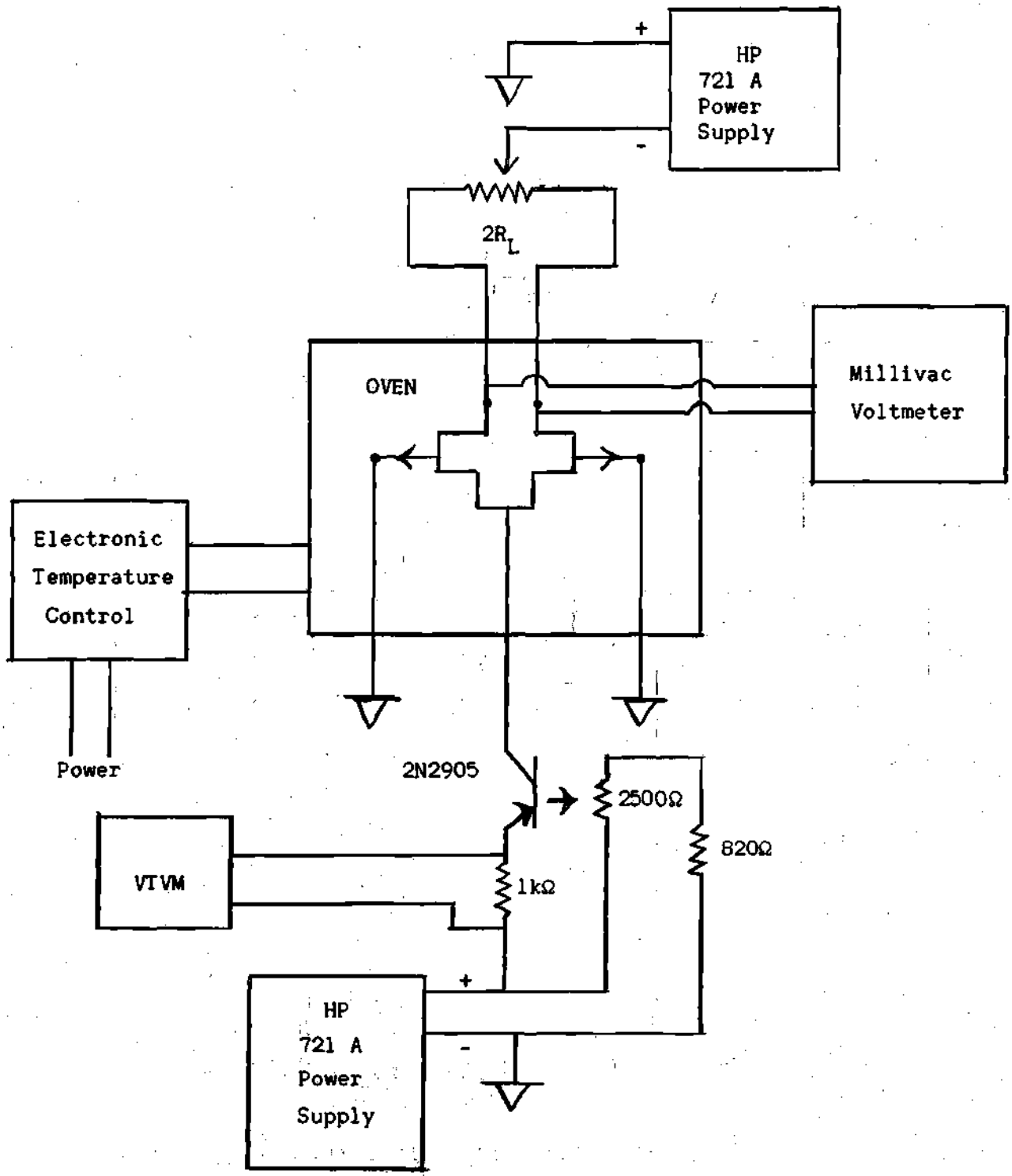
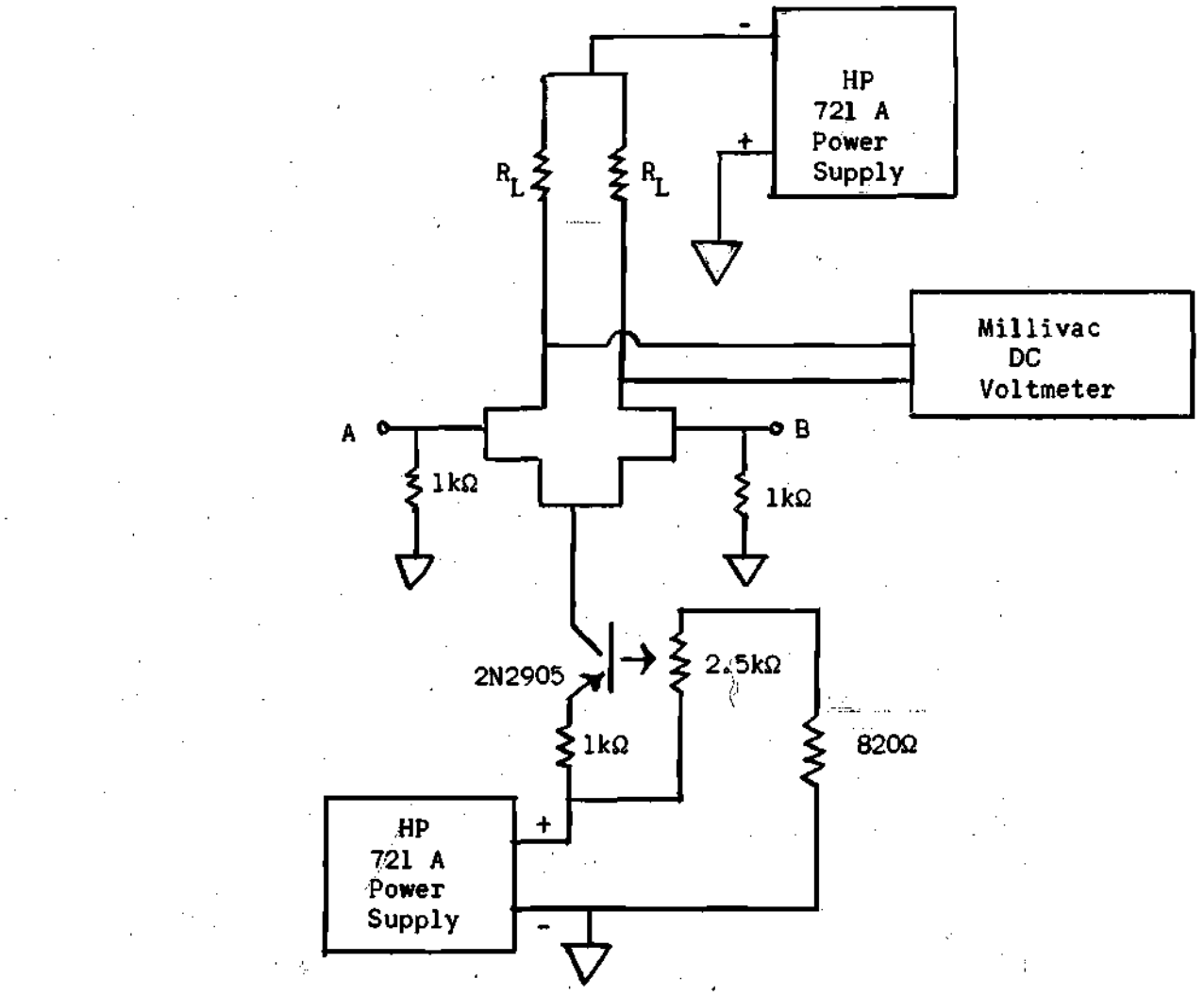


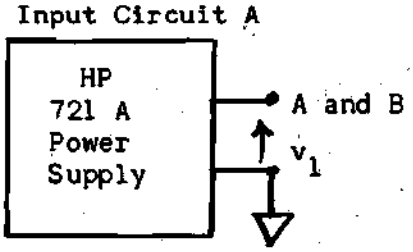
Figure 12. Equivalent Input Drift Measurement.

by ΔT, gives the equivalent input voltage drift per degree centigrade.

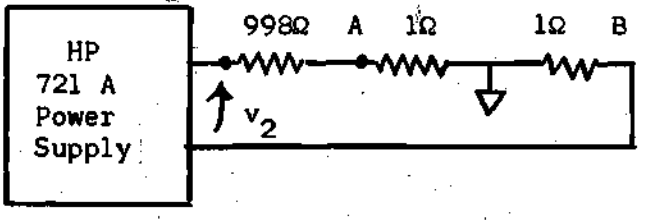
The equivalent input current drift per degree centigrade was not evaluated for the following reasons. The equivalent input current drift is due to the unbalance in the I_{GSS}'s, the gate-source leakage currents, and the difference in their changes with temperature. This drift is minimized simply by picking units which have equal I_{GSS} at a temperature much greater than the desired temperature of operation. These units should then have essentially equal values of I_{GSS} at the temperature of operation and should track well as the temperature changes.

The circuit that was used to measure common mode rejection is shown in Figure 13. Input Circuit A is connected as shown. This provides a completely common mode input to the amplifier. The power supply voltage V_1 is increased until the DM output can be measured with sufficient accuracy. These values are recorded and input circuit B is connected as shown. This provides a completely DM input to the amplifier. The measured DM output divided by $2V_2 \times 10^{-3}$ gives the DM gain. To calculate common mode rejection, the value of DM output, measured with input circuit A connected, is divided by the DM gain to give the DM input that would produce this output. Dividing V_1 by this value gives the common mode rejection factor.





Input for Measuring DM output for CM Input



Input for Measuring DM Output for DM Input

Figure 13. Common Mode Rejection Measurement Circuit.

CHAPTER IV

DISCUSSION OF RESULTS

The drift constants k and c, V_p, and I_{DSS} for 10 FET's are tabulated in Table 1. The table also includes the predicted values of quiescent drain current for minimum change with temperature calculated by Equations 9 and 15 along with the experimentally measured values of quiescent drain current that gave minimum drift. It is seen that, for FET's with V_p less than about two volts, the agreement between the predicted and measured values of drain current for minimum drift is quite good. For those units with V_p greater than two volts the equations predict a value which is somewhat larger than the actual value, which tends toward zero drain current. It is also to be noted that Equation 9 seems to give a better estimate than Equation 15.

There are several reasons why the predicted value of minimum drift drain currents lies above the actual value as V_p increases. As V_p increases, it is seen from the last part of chapter two that k and c are converging to a common value since

$$c \approx k + \frac{2 \times 10^{-3}}{V_p} .$$

Equation 9 gives the value of quiescent drain current for minimum drift as:

$$I_D = I_{DSS}\Big|_{T\ ref} 4 \left(\frac{k - c}{2c - k}\right)^2$$

Table 1. Predicted and Experimental Values of Quiescent Drain Current for Minimum Change with Temperature

Sample	I_{DSS} 22°C	V_p Volts	Predicted I_D - 22°C ma	Predicted I - 22° C ma	Experimental I_D - 22°C ma	$k \times 10^{-3}$	$c \times 10^{-3}$
2N2386-1	7.3	6.4	.174	.11	.002	4.54	4.18
2N2386-2	1.62	2.3	.058	.086	.001	4.19	4.68
2N2386-3	1.37	2.75	.0137	.076	.00	4.68	4.465
2N2386-4	0.95	1.37	.149	.168	.11	3.75	4.97
2N2386-5	3.31	3.1	.067	.110	.01	5.77	6.25
2N2386-6	.92	1.65	.0032	.15	.004	3.5	3.61
2N2386-7	.79	1.63	.05	.126	.025	3.58	3.22
2N2386-A	1.34	1.75	.18	.28	.135	3.75	4.575
2N2386-B	1.97	1.87	.264	.176	.2	5.04	6.5
2N2386-C	2.08	2.02	.12	.196	.14	4.48	5.18

For large V_p where $k \simeq c$ it is seen that a small error in the measurement of k or c has little effect on the denominator of the term in parenthesis but can cause a large error in the numerator which is compounded when the expression is squared. The fact that equation 9 is more accurate than equation 15 for large V_p devices justifies the above reasoning. In Chapter II c was derived from the temperature dependence of I_{DSS} and V_p to be equal to

$$\left(k + \frac{2 \times 10^{-3}}{V_p} - \frac{k^2 \times 10^{-3}}{V_p}\right)$$

which is approximately

$$k + \frac{2 \times 10^{-3}}{V_p}$$

As V_p increases and the values of k and c converge, however, neglecting the third term can introduce considerable error. In calculating c from equation 9, a straight line was drawn from g'_{fs} at 22°C to g'_{fs} at 50°C and slope of this line was taken to be c. This is equivalent to calculating c as

$$k + \frac{2 \times 10^{-3}}{V_p} - \frac{k2 \times 10^{-3}}{V_p} \tau$$

and letting τ = 28°C. This yields a smaller value of c than letting

$$c = k + \frac{2 \times 10^{-3}}{V_p}$$

which reduces equation 9 to equation 15. With c smaller, $k - c$ is smaller which becomes significant as k and c converge and, therefore, equation 9 predicts a lower value of quiescent drain current than equation 15.

It is seen from equations 9 and 15 that as V_p increases, the value of I_D for minimum drift is decreasing approximately as $(1/V_p)^2$. Thus, the value of I_D yielding minimum drift for the units with larger V_p is a much smaller percentage of I_{DSS} than the lower V_p units. Temperature sensitive leakage currents were neglected in the basic equations given for the FET. With large V_p units where I_D for minimum drift is getting quite small, these leakage currents can cause appreciable error at these low levels.

In general, it may be said that these formulas give reasonable accuracy in predicting the value of drain current for minimum drift with the predicted value diverging above the actual value as V_p increases above approximately two volts.

In Table 2 the equivalent input voltage drift for a differential stage using those units which were the most closely matched is tabulated. Drifts in the range of 100 μ volts/°C were achieved which is quite good considering the quality of the matching. It is noted that the equivalent input drift does not necessarily increase as I_D increases above the level of the minimum drift values. This is reasonable since g_{fs} increases as I_D increases. Although the change in I_D with temperature increases as quiescent I_D increases above the minimum drift value, the equivalent input drift does not necessarily change because the equivalent input drift is $\Delta I_D/g_{fs}$ and g_{fs} increases with I_D. It is to be noted that the equivalent input drift increases as both drain currents move below their minimum drift values because the change in I_D with temperature is increasing while g_{fs} is decreasing.

In Chapter I the common mode rejection factor for a differential stage using FET's at low values of I_D was shown to approach infinity as r_p and R approach infinity. For large, but finite, r_p and R the rejection factor should be large for such a stage. This was verified experimentally and the results are tabulated in Table 3. Common mode rejection factor values approaching 10^4 were achieved which is quite good for this simple configuration and the degree of matching. The rejection factor in general increased as I_D decreased which is in agreement with the theory since r_p varies inversely with I_D.

Table 2. Equivalent Input Drift for FET Differential Stage

Specimens B and C - 2N2497

I_D ma	Vin µv/°C
.1	340
.25	365
.5	235
1.0	255
1.5	165

Specimens 4 and 6 - 2N2386

I_D ma	Vin µv/°C
.1	1500
.2	1090
.4	475
.6	404
.8	264

Specimens 6 and 7 - 2N2386

I_D ma	Vin µv/°C
.1	650
.25	145
.4	186
.6	76.5
.7	169

Table 3. Common Mode Rejection Factor for Differential Stage Using FET's - 2N2497 Specimens B and C

Specimens B and C - 2N2497

I_D ma	CM Rejection Factor
.3	2.15×10^3
.2	5.0×10^3
.1	2.5×10^3
.05	7.15×10^3

CHAPTER V

CONCLUSIONS AND RECOMMENDATIONS

Two of the advantages, listed in Chapter I, of using the FET in a differential stage were its low noise properties and high input impedance capabilities. It has also been shown theoretically and verified experimentally in this report that the FET also has the following two advantages:

1. The FET differential stage is capable of high common mode rejection.

2. There is a value of quiescent drain current, which can be predicted reasonably well, at which the change of I_D with temperature is a minimum. Therefore, the equivalent input drift of a FET differential stage can be minimized, not only by matching the two FET's but also by proper selection of the operating point.

In order to maximize performance in a FET differential stage, it is recommended that one use well matched FET's with V_p between two and three volts. There are several reasons for recommending the higher V_p units. For the higher V_p units the predicted value of I_D for minimum change with temperature is a much smaller percentage of I_{DSS} and lies above the actual value giving minimum drift. Since I_D is small, r_p can be quite large since r_p varies inversely with I_d. Increasing r_p improves the common mode rejection ratio.

The maximum possible gain varies inversely with $\sqrt{I_D}$. The maximum

possible gain occurs when R_L approaches infinity and thus is $g_{fs}\, r_p$. From equations 1, 2, and 3, it is seen that g_{fs} decreases as the square root of I_D/D_{SS} whereas, as stated above, r_p increases inversely with I_D/I_{DSS}. Therefore, the maximum possible gain increases inversely as the square root of I_D/I_{DSS}. To illustrate the above, assume $I_D = 0.1\ I_{DSS}$ for a particular FET. Then $r_p = 10\ r_p'$ where r_p' is the value of r_p for V_{GS} equal to zero, whereas g_{fs} equals $\sqrt{.1}\, g_{fs}'$ or $0.316\ g_{fs}'$. The maximum possible gain, therefore, is $g_{fs}\ r_p$ which equals $(.316\ g_{fs}')(10\ r_p')$ or 3.16 times maximum possible gain at $I_D = I_{DSS}$.

Since the predicted value of I_D for minimum drift seems to be always above the actual value for the larger V_p units, operation at the predicted value ensures that both FET's will be above their actual values for minimum drift. Therefore, both will be attempting to change in the same direction and the large common source impedance will produce feedback to offset the attempted changes. It has also been shown that the equivalent input drift does not necessarily increase as I_D increases above the minimum drift value due to the increase in g_{fs}. If the operating point is chosen such that one FET is slightly above its minimum drift value and the other slightly below, then the changes with temperature are in opposite directions or differential and the large common source impedance is ineffective in producing feedback.

Thus, with the larger V_p units one can operate at small values of drain current and still be above the minimum drift values which improves gain, common mode rejection, and equivalent input drift.

It is also recommended that equation 15 be used instead of equation

9 to predict I_D for minimum drift. For lower V_p units, they predict about the same values of I_D, whereas for the larger values of V_p they both predict above the actual value of I_D for minimum drift, which is advantageous as discussed above. Equation 15 requires the measurement of only one drift parameter k which is quite easy to measure, whereas, equation 9 requires more complex measurements. To refrain from making temperature measurements, one can use an average value of k in equation 15 and would only have to know V_p to predict the value of I_D/I_{DSS} for minimum drift. This should result in a loss of accuracy, but would require minimum time and measurements.

APPENDIX

Note: Statistical average of experimental data for a sample of 10 FET's

Table 4. Average Data for 2N2386 - Specimen 1

I_D ma T = 22°C	I_D ma T = 50°C	V_{GS} volts
7.37	6.42	0
6.66	5.827	.3
6.02	5.525	.6
5.42	4.727	.9
4.85	4.22	1.2
4.29	3.73	1.5
3.77	3.267	1.8
3.26	2.82	2.1
2.79	2.407	2.4
2.35	2.02	2.7
1.95	1.68	3.0
1.24	1.067	3.6
.68	.58	4.2
.31	.27	4.8
.14	.12	5.4
.0685	.059	6.0
.019	.00174	7.0
.002	.002	8.0

Table 5. Average Data for 2N2386 - Specimen 2

I_D ma T = 22°C	I_D ma T = 50°C	V_{GS} volts
1.62	1.43	0
1.18	1.05	.3
.82	.73	.6
.53	.477	.9
.31	.288	1.2
.18	.16	1.5
.121	.112	1.8
.102	.09	2.1
.09	.076	2.4
.076	.063	2.7
.063	.0525	3.0
.043	.037	3.6
.0274	.023	4.2
.0165	.0134	4.8
.0084	.006	5.4
.003	.002	6.0

Table 6. Average Data for 2N2386 - Specimen 3

I_D ma T = 22°C	I_D ma T = 50°C	V_{GS} volts
1.37	1.19	0
1.05	.91	.3
.79	.68	.6
.577	.495	.9
.41	.35	1.2
.287	.24	1.5
.20	.167	1.8
.137	.11	2.1
.081	.07	2.4
.05	.042	2.7
.029	.025	3.0
.01	.0084	3.6
.0047	.0032	4.2
.0016	.001	4.8

Table 7. Average Data for 2N2386 - Specimen 4

I_D ma T = 22°C	I_D ma T = 50°C	V_{GS} volts
.95	.85	0
.57	.52	.3
.29	.27	.6
.11	.1075	.9
.021	.022	1.2
.0063	.0053	1.5
.0021	.001	1.8
.001		2.1

Table 8. Average Data for 2N2386 - Specimen 5

I_D ma T = 22°C	I_D ma T = 50°C	V_{GS} volts
3.31	2.79	0
2.62	2.26	.3
2.08	1.795	.6
1.60	1.39	.9
1.187	1.03	1.2
.83	.72	1.5
.54	.47	1.8
.32	.28	2.1
.17	.15	2.4
.10	.08	2.7
.067	.057	3.0
.043	.036	3.6
.031	.0253	4.2
.023	.0188	4.8
.0169	.0134	5.4
.011	.0105	6
.005	.005	7
.0018	.0018	8

Table 9. Average Data for 2N2386 - Specimen 6

I_D ma T = 22°C	I_D ma T = 50°C	V_{GS} volts
.92	.83	0
.58	.525	.3
.33	.30	.6
.18	.16	.9
.10	.085	1.2
.0464	.042	1.5
.023	.021	1.8
.0105	.0095	2.1
.0042	.0042	2.4

Table 10. Average Data for 2N2386 - Specimen 7

I_D ma T = 22°C	I_D ma T = 50°C	V_{GS} volts
.79	.71	0
.50	.45	.3
.29	.267	.6
.16	.14	.9
.07	.065	1.2
.0253	.0253	1.5
.0071	.0071	1.8
.0016	.0018	2.1

Table 11. Average Data for 2N2497 - Specimen A

I_D ma T = 22°C	I_D ma T = 50°C	V_{GS} volts
1.34	1.20	0
.92	.83	.3
.575	.53	.6
.317	.297	.9
.135	.135	1.2
.0384	.04	1.5
.0136	.0126	1.8
.0095	.0084	2.1
.0068	.0063	2.4
.005	.0042	2.7
.0031	.0031	3.0

Table 12. Average Data for 2N2497 - Specimen B

I_D ma T = 22°C	I_D ma T = 50°C	V_{GS} volts
1.97	1.69	0
1.35	1.21	.3
.897	.81	.6
.53	.49	.9
.26	.25	1.2
.08	.084	1.5
.0084	.0105	1.8
.001	.0016	2.1

Table 13. Average Data for 2N2497 - Specimen C

I_D ma T = 22°C	I_D ma T = 50°C	V_{GS} volts
2.08	1.82	0
1.47	1.33	.3
1.01	.92	.6
.63	.58	.9
.34	.32	1.2
.14	.14	1.5
.036	.039	1.8
.0095	.01	2.1
.0032	.0037	2.4
.001	.0018	2.7

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